Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A circuit, comprising:
circuit elements;
scan chain elements to contain a vector for selective application to said circuit elements;
a vector memory for containing a configuration vector which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;
a multiplexer to select said configuration vector for loading into said scan chain elements; and
a clock generator to clock said configuration vector into said scan chain elements.

[c2] 2. The circuit of claim 1 further comprising a sleep mode detector to configure said multiplexer to select said configuration vector and to operate said clock generator to clock said configuration vector into said scan chain elements when a sleep mode of said circuit is detected.

[c3] 3. The circuit of claim 2 further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements.

[c4] 4. A circuit, comprising:
circuit elements;
scan chain elements to contain a vector for selective application to said circuit elements;
a circuit for receiving a test vector for clocking into said scan chain elements;
a vector memory for containing a configuration vector which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;
a multiplexer to select between said configuration vector and said test vector for loading into said scan chain elements; and
a clock generator to clock said selected vector into said scan chain elements.

[c5] 5. The circuit of claim 4 further comprising a sleep mode detector to configure said multiplexer to select said configuration vector and to operate said clock generator to clock said configuration vector into said scan chain elements when a sleep mode of said circuit is detected.

[c6] 6. The circuit of claim 5 further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements.

[c7] 7. A method for reducing leakage currents in a circuit, comprising:
clocking a configuration vector into scan chain elements for application to circuit elements within said circuit, wherein said configuration vector configures said circuit elements into a state in which leakage currents are reduced.

[c8] 8. The method of claim 7 further comprising detecting a sleep mode, and in response thereto performing said clocking.

[c9] 9. The method of claim 7 further comprising turning off clock pulses to said scan chain elements after said configuration vector has been applied to said circuit elements.

[c10] 10. A method for reducing leakage currents in a circuit, comprising:
selectively clocking either a test data vector or a configuration vector into scan chain elements for application to circuit elements within said circuit,
wherein when said configuration vector is clocked into said scan chain elements, said configuration vector configures said circuit elements into a state in which leakage currents are reduced.

[c11] 11. The method of claim 10 further comprising detecting a sleep mode, and in response thereto performing said clocking.

[c12] 12. The method of claim 10 further comprising turning off clock pulses to said scan chain elements after said configuration vector has been applied to said circuit elements.

[c13] 13. A method for reducing leakage currents in a circuit, comprising:
determining a vector having first states which if applied to circuit elements of said circuit results in lower leakage currents than second states;
detecting an operating mode of said circuit;
clocking said vector into scan chain elements of said circuit for application thereby to said circuit elements when said operating mode is detected.

[c14] 14. The method of claim 13 wherein said detecting an operating mode comprises detecting a sleep mode.

[c15] 15. The method of claim 13 further comprising turning off clock pulses to said scan chain elements after said vector has been applied to said circuit elements.

[c16] 16. A method for reducing leakage currents in a circuit,

comprising:

determining a configuration vector having first states which if applied to circuit elements of said circuit results in lower leakage currents than second states;

detecting whether said circuit is operating in either a first or a second operating mode;

clocking said configuration vector into scan chain elements of said circuit for application thereby to said circuit elements when said first operating mode is detected;

and clocking test data into said scan chain elements of said circuit for application thereby to said circuit elements when said second operating mode is detected.

[c17] 17. The method of claim 16 wherein said detecting a first operating mode comprises detecting a sleep mode.

[c18] 18. The method of claim 16 wherein said detecting a second operating mode comprises detecting a test mode.

[c19] 19. The method of claim 16 further comprising turning off clock pulses to said scan chain elements after said vector has been applied to said circuit elements.